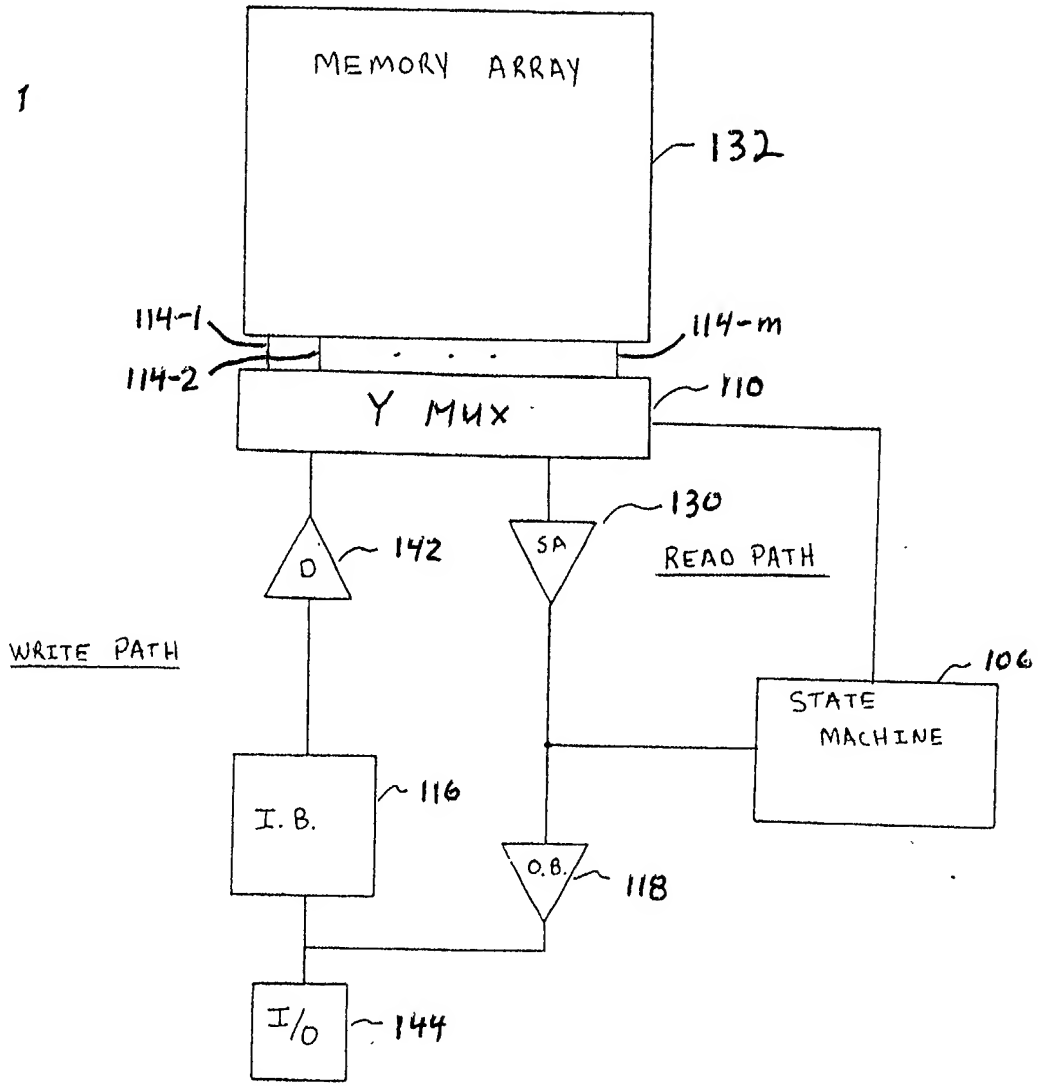
FIGURE 1

(PRIOR ART)



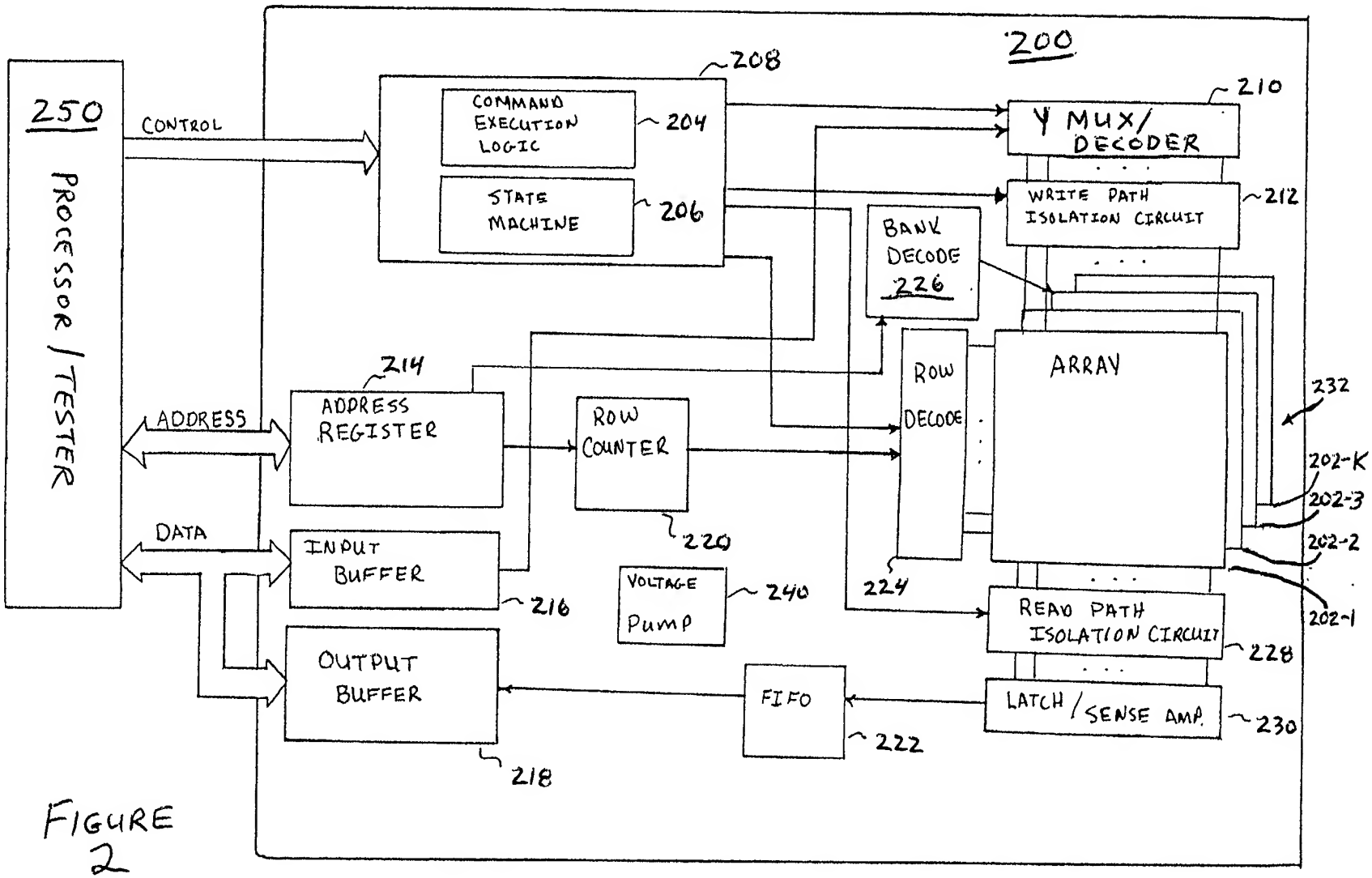
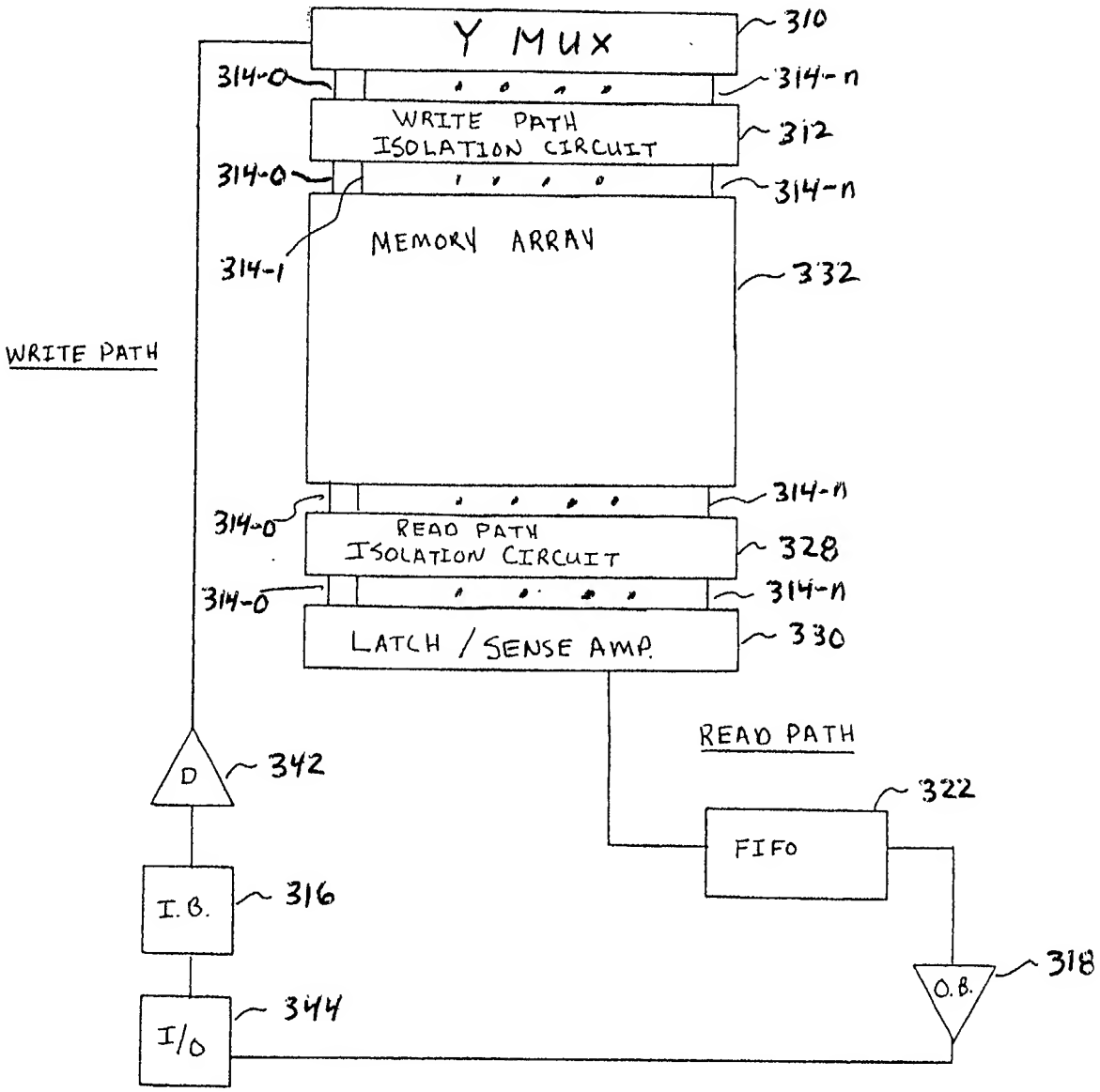

250
PROCESSOR / TESTER
CONTROL
ADDRESS
DATA
200
208
COMMAND EXECUTION LOGIC
204
STATE MACHINE
206
210
Y MUX/ DECODER
WRITE PATH ISOLATION CIRCUIT
212
BANK DECODE 226
ROW DECODE
ARRAY
232
202-K
202-3
202-2
202-1
214
ADDRESS REGISTER
ROW COUNTER
220
INPUT BUFFER
216
VOLTAGE Pump
240
224
READ PATH ISOLATION CIRCUIT
228
OUTPUT BUFFER
218
FIFO
222
LATCH / SENSE AMP.
230

FIGURE 2

FIGURE 3


Y MUX
310
314-0
314-n
WRITE PATH ISOLATION CIRCUIT
312
314-0
314-n
314-1
MEMORY ARRAY
332
WRITE PATH
314-n
314-0
READ PATH ISOLATION CIRCUIT
328
314-0
314-n
LATCH / SENSE AMP.
330
READ PATH
D
342
322
FIFO
I.B.
316
O.B.
318
I/O
344

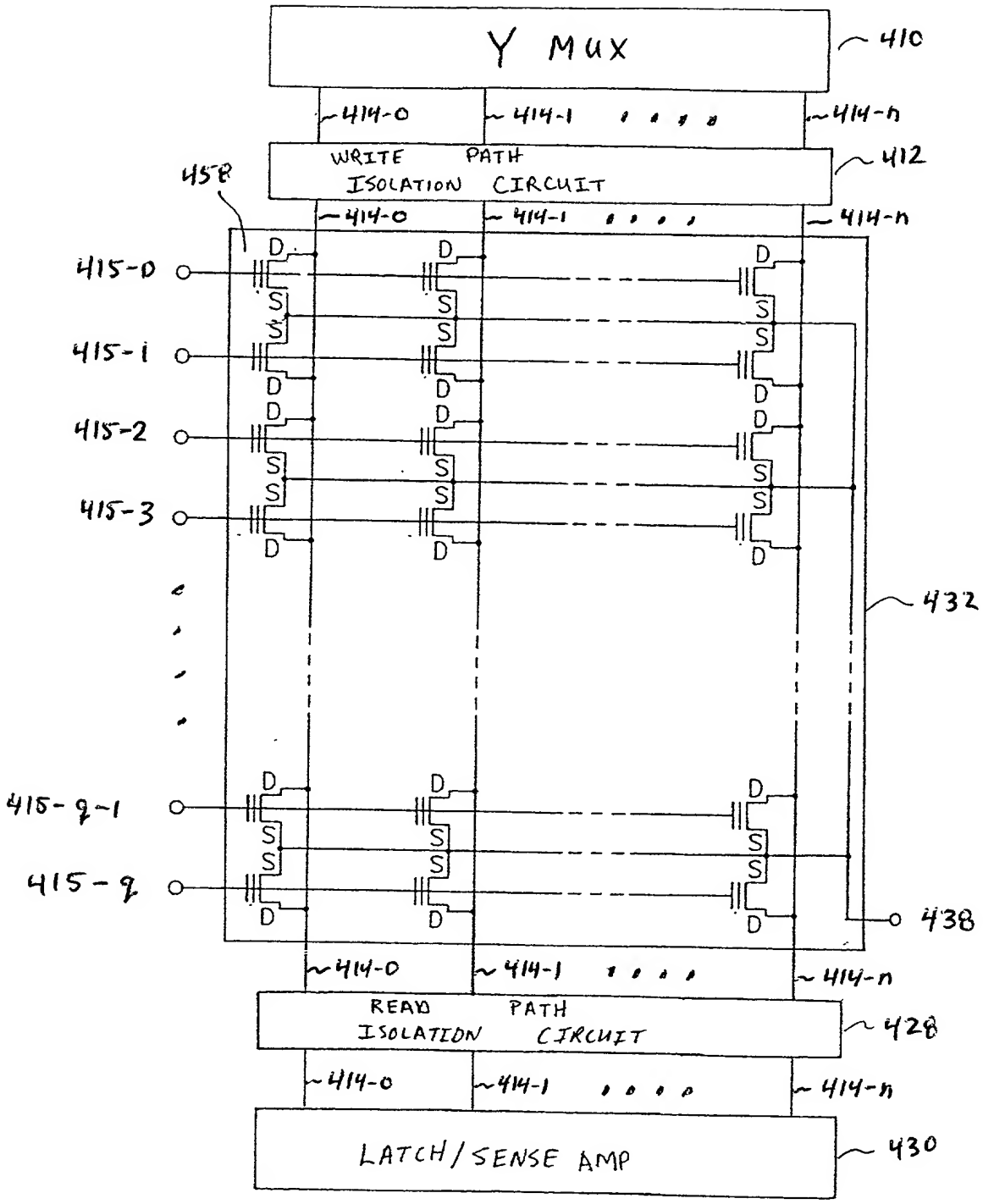
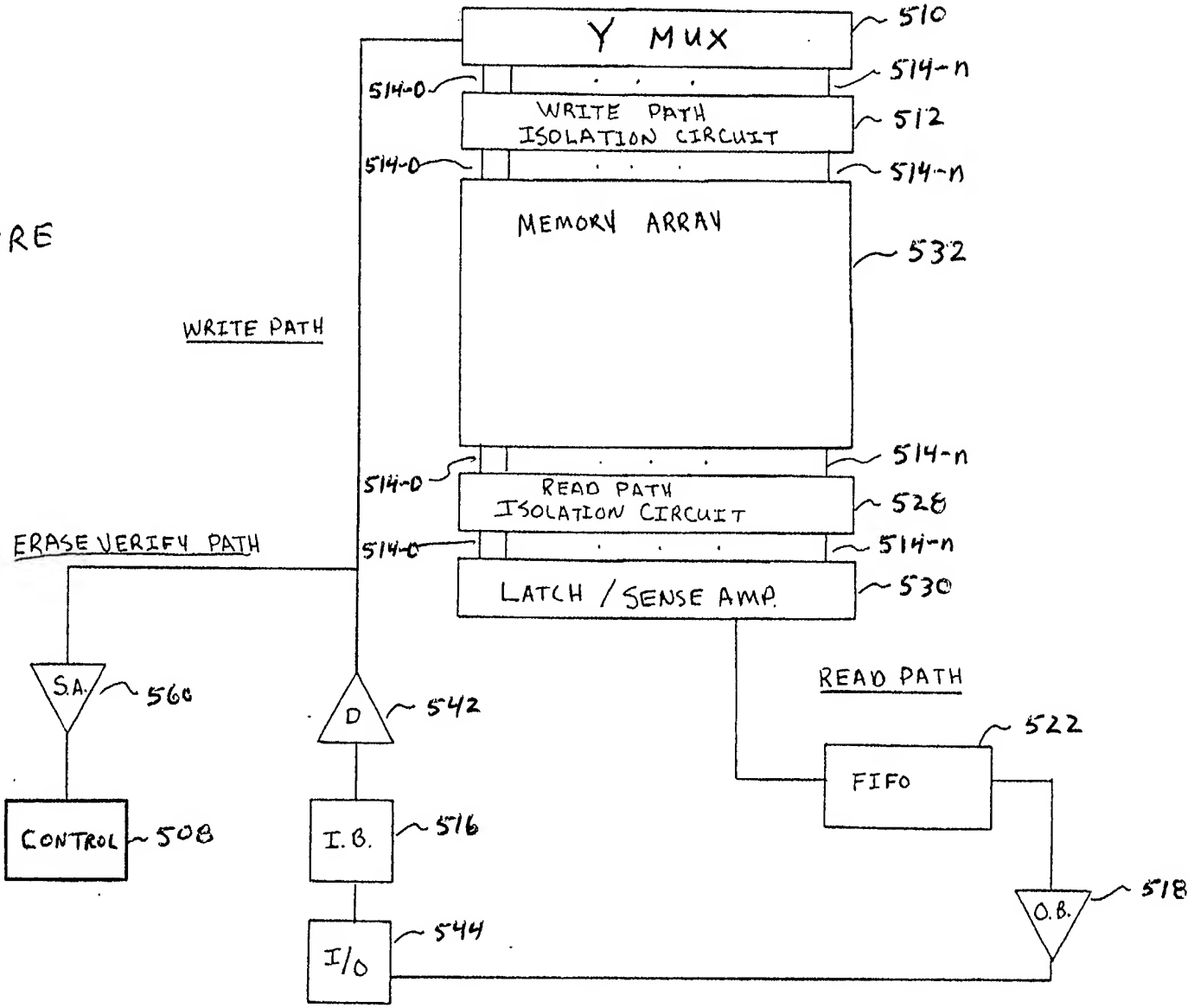

Y MUX
410
414-0
414-1
414-n
WRITE PATH ISOLATION CIRCUIT
412
458
415-0
415-1
415-2
415-3
415-q-1
415-q
D
S
432
438
READ PATH ISOLATION CIRCUIT
428
LATCH/SENSE AMP
430

FIGURE 4

FIGURE 5


Y MUX
510
514-n
514-0
WRITE PATH ISOLATION CIRCUIT
512
514-0
514-n
MEMORY ARRAY
532
WRITE PATH
514-n
514-0
READ PATH ISOLATION CIRCUIT
528
ERASE VERIFY PATH
514-0
514-n
LATCH / SENSE AMP.
530
READ PATH
S.A.
560
D
542
522
FIFO
CONTROL
508
I.B.
516
O.B.
518
I/O
544

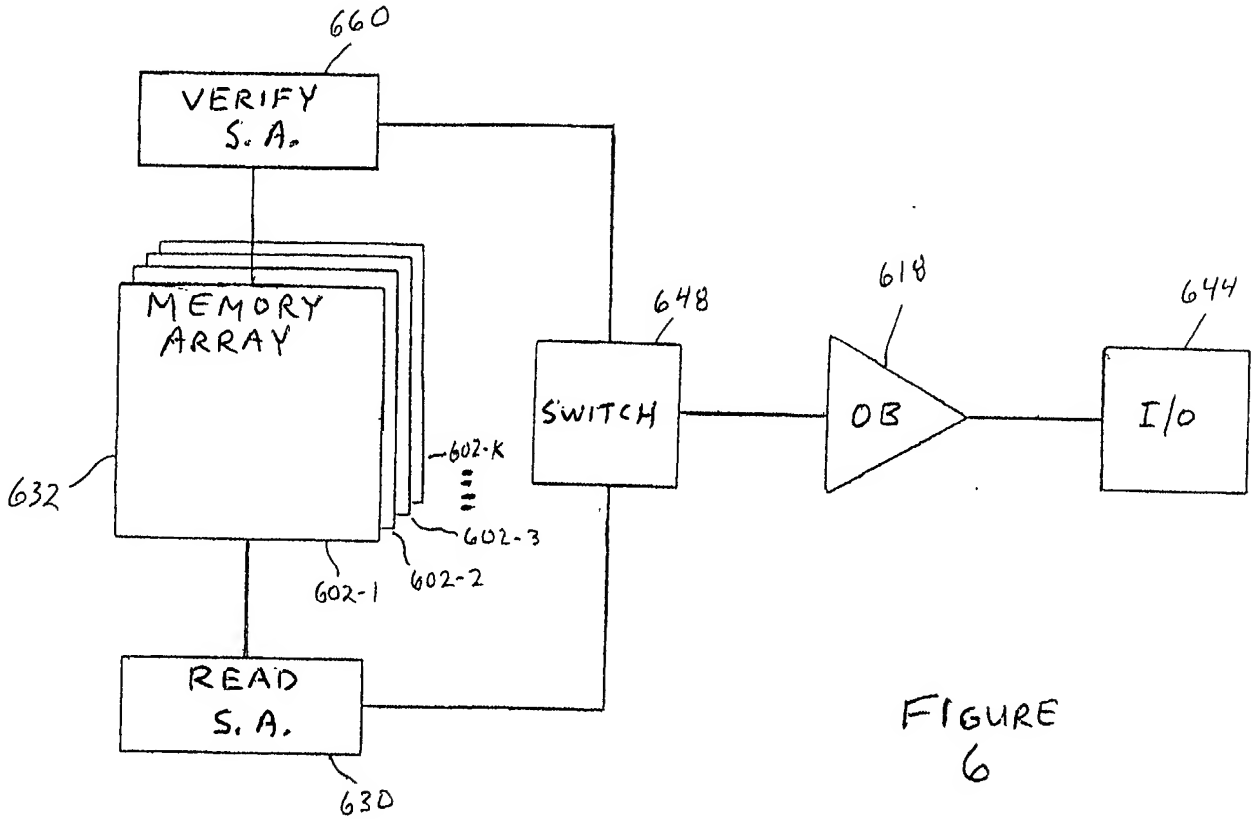
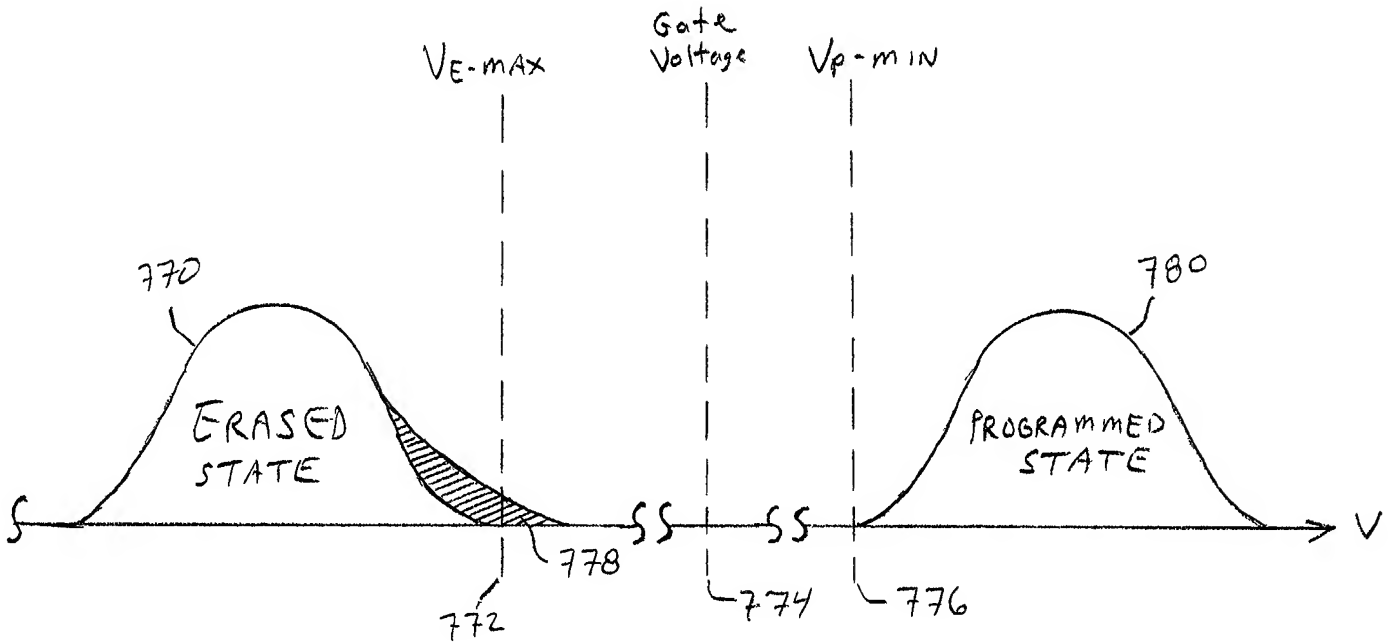

660
VERIFY
S. A.
MEMORY
ARRAY
632
602-K
602-3
602-2
602-1
READ
S. A.
630
648
SWITCH
618
OB
644
I/O

FIGURE
6

FIGURE 7


Gate Voltage
$V_{E\text{-}MAX}$
$V_{P\text{-}MIN}$
770
780
ERASED STATE
PROGRAMMED STATE
778
772
774
776
V

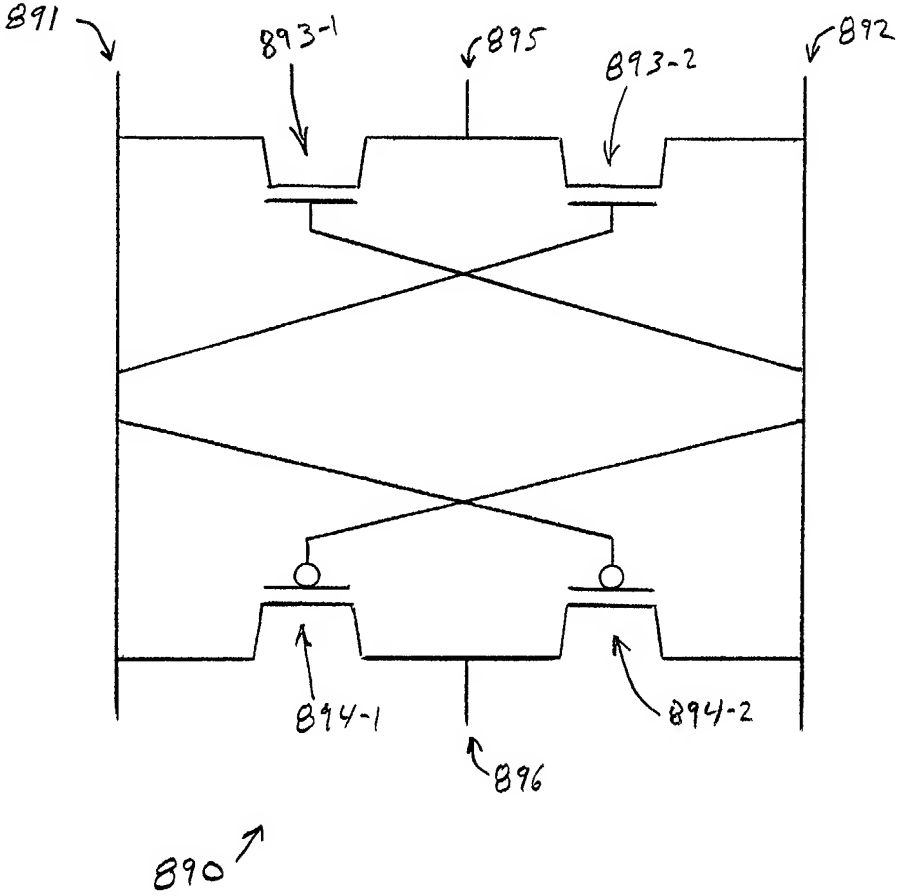


FIGURE 8
PRIOR ART